Amendments to the Specification:

Please replace the paragraph beginning at page 4, line 11 with the following rewritten paragraph:

Two functional units 14a,b, shown by way of example, are standard non-configurable functional units 14a,b such as an ALU (arithmetic-logic unit), or a memory load store unit etc. Functional unit 16 is a configurable functional unit. The processing device may contain more of such configurable functional units ~~14~~ 16, which is capable of receiving the instructions and performing operations on operands from register file 12, but by way of example only one configurable functional unit 16 is shown.

Please replace the paragraph beginning at page 4, line 26 with the following rewritten paragraph:

In operation, instruction issue unit 10 issues successive instructions to the functional units 14a,b, 16. (For this purpose, instruction issue unit 10 may contain for example an instruction memory, an instruction cache, a program counter, a branch unit etc. not shown in figure 1). The instructions may be issued in parallel to the functional units 14a,b 16, for example in case of a VLIW or superscalar type of architecture or in series, in which case instruction issue unit 10 selects which of the functional units 14a,b, 16 has to execute the instructions. Functional units 14a,b, 16 pass operand and result register selection codes from the instructions to the their ports to register file 12 (the ports may be shared among a set of different functional units 14a,b 16, as long as only one of the set accesses the register file 12 at a time). Functional units 14ab, 16 execute the instructions that they are ordered to execute by the instruction issue unit 10, using operands ~~form~~ from the register file 12 as addressed by the instructions and writing results to the register file 12 as specified in the instructions.